REMARKS

Pending Claims

Claims 12-13, 15, 18-20, and 26 are currently pending. Claims 12, 13, 15, 18, 19, 20, and 26 are currently amended. Claims 14, 16, 17, and 21-25 are cancelled herewith. Claims 1-11 were previously cancelled. Support for the amendments to claim 12 can be found at least in Fig. 1. Claim 13 has been amended to incorporate the language of claim 14. Claim 15 has been amended to incorporate the language of claim 16. No new matter is added.

Rejections Under 35 U.S.C. § 103

Claims 12-16 and 24-26 stand rejected under 35 U.S.C. § 103(a) as being obvious over the combination of what the Examiner has identified as the Applicant Admitted Prior Art ("AAPA") in view of Miyashita et al. (USP 5,610,954). In addition, claims 19-22 stand rejected under 35 U.S.C. § 103(a) as being obvious over the combination of the AAPA in view of Miyashita et al. further in view of Yonekura et al. (USP 5,761,617). Further, claims 17-18 stand rejected under 35 U.S.C. § 103(a) as being obvious over the combination of the AAPA in view of Miyashita et al. further in view of Anumula et al. (USP 6,566,967). Finally, claim 23 stands rejected under 35 U.S.C. § 103(a) as being obvious over the combination of the AAPA, Miyashita et al., Anumula et al. and further in view of Yonekura et al. However, in view of the amendments and arguments presented herein, Applicant respectfully submits that the rejections have been traversed and request that the rejections be reconsidered and withdrawn.

The combinations of references cited by the Examiner fail to render the claims obvious because none of the combinations of references teaches or suggests all of the elements of the claimed combinations. Among other distinctions, the AAPA does not teach or suggest a clock and data recovery circuit which includes a phase detector circuit that detects a phase difference between a received data signal and a discriminated data signal that has been discriminated and output by a discriminator circuit, as recited in claims 12, 13, and 15.

Instead, the phase detector circuit 910 in the AAPA (Fig. 11 of the present application) detects a phase difference between an input data signal (DATA IN) and an output signal (Clock

Out) of the variable delay circuit 912. The output of the phase detector circuit 910 is supplied via a low pass filter to the variable delay circuit 912. The AAPA neither teaches nor suggests a configuration in which (1) a phase difference between a discriminated data signal (discriminated by a discriminator circuit) and a received data signal is detected and (2) an integrated signal of the phase difference is supplied to the phase shifter which shifts a phase of an oscillation clock signal to supply the shifted clock signal to the discriminator circuit as a discrimination clock signal.

Miyashita fails to supply the deficiencies of the AAPA. In Fig. 7 of Miyashita the complementary clock signals CLK and *CLK output from VCO 50 are directly supplied to the clock terminals (labeled CK) of the discriminator circuits (D-FFs) 21A and 21B, respectively. Further, the output of element 22A (an EXOR element) is supplied to a non-inverting input terminal (labeled "+") of differential amplifier 32. The output of the differential amplifier 32 is connected to an input of the VCO 50 as well as to an inverting input terminal (labeled "-") via a capacitor and a resistor connected in series (i.e. a smoothing, or integrator, circuit). Thus, a feedback loop in Fig. 7 of Miyashita includes: discriminator 21A, 21B -> phase comparator 22A -> integrator -> VCO 50 -> "clock in" of the discriminator. That is, in Fig. 7 of Miyashita the resulting phase comparison output by element 22A is not supplied to a phase shifter, as recited in the present claims, but instead is supplied to a differential amplifier.

Miyashita does not disclose providing a phase shifter which shifts a phase of a clock signal output from the VCO, based on an integrated phase comparison result between a discriminated data signal output by a discriminator and a received data signal, where the clock that is output from the phase shifter is supplied to the discriminator as a discrimination clock.

While the Examiner cites to particular elements from the claims that are allegedly present in the cited references, many of the elements, in particular those relating to how the elements are interconnected, are not taught in the references. Instead, the Examiner appears to be using impermissible hindsight to reject the claims, using the claim language as a roadmap for the rejection. Given that electrical circuits are typically constructed by assembling known elements in new ways, the connections between the elements are often what make the circuit inventive. Thus, in rejecting the present claims it is insufficient for the Examiner to list the individual

elements that are taught by the references without indicating how the references teach or suggest the particular arrangement of components that is claimed. As mentioned above, among the elements that the Examiner fails to identify are a phase detector, the output of which serves as an input to a phase shifter, where the output of the phase shifter in turn is a clock signal for the discriminator. The Examiner argues that element 22A in Fig. 7 of Miyashita teaches a phase detector such as that claimed. However, the output of element 22A feeds into a voltage-controlled oscillator (VCO) 50, not a phase shifter. Thus, there is no teaching or suggestion in Miyashita to have the output of the phase detector serve as input to the phase shifter, as recited in the claims.

The Examiner argues that the element of claim 12 which recites "wherein the discriminator circuit, the phase detector circuit, and the phase shift circuit comprise a feedback loop separate from the phase synchronization loop" is obvious because this amounts to "making separable" as described in MPEP 2144.04(V). In particular, the Examiner argues that this element amounts to "only taking one piece of circuitry and separating it into two pieces of circuitry." However, as explained in the specification (e.g. p. 22, line 18 through p. 25, line 24), the use of two separate feedback loops permits features such as the clock oscillation frequency and the clock phase to be controlled independently of one another, permitting, for example, a quicker response to changes in the data signal than changes in the clock signal. Thus, having separate feedback loops serves a particular purpose and is more than simply "making separable" and is thus non-obvious.

Thus the combination of the AAPA in view of Miyashita et al. fails to render obvious any of independent claims 12, 13, or 15.

For at least the reason that each depends from an allowable independent claim and because each recites additional patentable subject matter, dependent claims 18-20 and 26 are also patentable.

CONCLUSION

In view of the remarks and amendments presented herein, reconsideration and withdrawal of the pending rejections and allowance of the claims are respectfully requested. The Examiner is strongly encouraged to contact the undersigned at the phone number below should any issues remain with respect to the application.

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